REMARKS

Claims 1-25 are pending. Claims 1, 12, 17, and 24 are independent claims. Claim 12 has been amended. Reconsideration and allowance of the above-referenced application are respectfully requested.

The specification stands objected to for failing to include a summary section. This objection is respectfully traversed. The cited rule states what a specification should include, and falls short of making a summary section mandatory. Intel Corporation has taken the position that they prefer to omit summaries in their applications. Since compliance with Rules 73 and 77 is entirely voluntary, it is respectfully suggested that the application is totally complete without a summary section, and therefore the requirement for a summary section is respectfully traversed.

The objection to claim 9 is respectfully traversed. As described in the specification (paragraph 0047), "The routing matrix 300 includes a row 320 that identifies which routing identifiers are to be used for routing a packet. The row 320 stores Boolean TRUE/FALSE values. Additional rows 325 also may be included in the routing matrix 300. These additional rows 325 may store additional information concerning the routing identifiers and how they are to be used during routing a packet.

This additional information also may be stored as Boolean TRUE/FALSE values. When all the elements of the routing matrix are Boolean TRUE/FALSE values, the routing matrix may be stored as a bit map, for example, as a single binary number." All the elements of the routing matrix may be stored as Boolean TRUE/FALSE values, i.e., 1 or 0. When all the elements of the routing matrix are either 1 or 0, this series can be stored as a single binary number. Thus, the routing matrix consists of a binary number. In view of the above, withdrawal of the objection to claim 9 is respectfully requested.

Claims 1-4, 7-9, 17-19, 24, and 25 are rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Cheriton et al. (US 6,091,725), hereinafter "Cheriton". Claims 5, 6, 12-16, and 20 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Cheriton. Claims 10, 11, and 21-23 are rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Cheriton in view of admitted prior art (AAPA), hereinafter "AAPA". These contentions are respectfully traversed.

Independent claim 1 reads, "receiving a routing address comprising at least two routing identifiers, and building a routing matrix to use in determining route identification operations to be performed, the routing matrix identifying one or more of the at least two routing identifiers that are to be

used in routing." Cheriton fails to describe or suggest features recited in claim 1.

Cheriton describes a technique for processing network datagram packets in network devices based on the source-destination address pair contained in the datagram packet itself (col. 4, lines 58-61). Datagram packets received on an input port are buffered in the shared memory buffer. The source-destination address pair in the datagram packet header is used to index the virtual path cache to find a matching entry. If a matching entry is found in the virtual path cache, then the switch hardware performs all the packet processing steps indicated in the virtual path record, including traffic management and packet routing. If no matching entry is found in the virtual path cache, then the datagram packet is forwarded to the controller CPU for general purpose processing. The controller CPU determines how to process further datagram packets with this source-destination address in the switch hardware. The controller CPU then loads an appropriate entry into the virtual path cache. See col. 5, lines 30-46.

Cheriton does not describe or suggest building a routing matrix to use in determining route identification operations. The cited portion of Cheriton (col. 11, lines 41-42) recites, in part, a method of combining source address information and

destination address information to determine an index value, and checking said table of routing information for an entry matching said index value. Thus, the table of routing information is not built by identifying one or more of the at least two routing identifiers that are to be used in routing, as recited in claim 1.

Further, Cheriton describes that datagram packets arriving through network ports 401 through 404 are temporarily stored in shared buffer memory 410. As soon as the datagram packet header has arrived, the virtual path cache is looked up to check whether a virtual path cache entry exists for this path. See, e.g., figure 4, col. 8, lines 32-38. Thus, the routing address is used to check whether a virtual path cache entry exists, not to build a virtual path cache entry. Since Cheriton describes combining source and destination address information and checking a table of routing information, Cheriton does not describe or suggest building a routing matrix to use in determining route identification operations to be performed, as recited in claim 1. Accordingly, claim 1 should be allowable. Dependent claims 2-11 should also be allowable at least for the above reasons and the additional recitations that they contain.

For example, claim 5 relates to a method of comparing the destination address to a source address to build a routing

matrix to use in determining route identification operations, wherein comparing the destination address comprises using blocks smaller than a length of a shortest of the two or more routing identifiers. Cheriton does not describe or suggest building a route identification matrix as discussed above. Accordingly, claim 5 should be allowable. Claim 6 should also be allowable at least for the above reasons.

Independent claim 12 reads, "receiving a source address and a destination address, each comprising at least two routing identifiers, performing an EXCLUSIVE OR operation of the source address routing identifiers with the destination address routing identifiers to produce an address comparison result, and determining a set of route identification operations to perform based upon one or more non-zero values in the address comparison result, wherein a different route identification operation is to be used for each of the one or more non-zero values."

Claim 12 recites features that cause a machine to determine route identification operations to perform based upon one or more non-zero values in the address comparison result, wherein a different route identification operation is to be used for each of the one or more non-zero values. In contrast, in Cheriton, the specific hash function logic is the bitwise Exclusive-OR between the low-order 15 bits of the destination address and the

source address of the virtual path index, producing the 15 bit virtual path cache index (figure 7, col. 9, lines 52-56). The virtual path cache index looks up the four parallel sets of the virtual path cache SRAMs. The tag field from each set of SRAMs is compared against the virtual path index and only that virtual path record that matches will be output on the virtual path record databus. See, e.g., col. 9, lines 34-43. Thus, in Cheriton, the result of the Exclusive-OR operation between the destination and the source address is compared against the virtual path index. Cheriton does not describe or suggest determining route identification operations based upon one or more non-zero values in the address comparison result.

Since Cheriton describes using the result of the Exclusive-OR operation to produce a virtual path cache index, and comparing the virtual path cache index against the four parallel virtual path cache SRAMS, Cheriton does not describe or suggest features of claim 12. Accordingly claim 12 should be allowable. Dependent claims 13-16 should also be allowable at least for the above reasons and the additional recitations that they contain.

Independent claim 17 relates to a system including a processor, a network device, a first bus, a memory system, and a second bus. The memory system embodies information indicative of instructions to cause the processor to perform operations

comprising receiving a source address and a destination address, each comprising at least two routing identifiers, and determining a set of route identification operations to perform based upon one or more differences between the source address routing identifiers and the destination address routing identifiers. Cheriton does not describe or suggest features of claim 17.

The portion cited by the Office Action (col. 9, lines 34-43) describes that the virtual path index enters the hash function which produces a virtual path cache index which in turn looks up the four parallel sets of the virtual path cache SRAMs. The tag field from each set of SRAMs is compared against the virtual path index and only that virtual path record that matches will be output on the virtual path record databus. The result of the logical operation performed on the destination and source addresses is used to determine whether or not the virtual path index of the incoming datagram exists in the virtual path cache SRAMs. See, e.g., col. 9, lines 34-43. Thus, the result of the logical operation is not used to determine a set of route identification operations.

Since Cheriton describes comparing the virtual path index of the incoming datagram against the virtual path cache SRAMs, and not determining a set of route identification operations to

be performed, Cheriton does not describe or suggest features of claim 17. Accordingly, independent claim 17 should be patentable. Independent claim 24 recites features similar to claim 17 and should be patentable at least for the same reasons. Dependent claims 18-23 and 25 should also be allowable at least for the above reasons and the additional recitations that they contain.

CONCLUSION

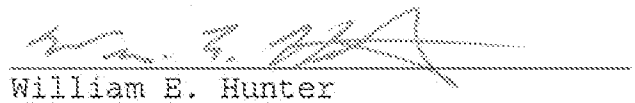
It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper.

It is respectfully suggested for all of these reasons, that the current rejection is totally overcome; that none of the cited art teaches or suggests the features which are claimed, and therefore that all of these claims should be in condition for allowance. A formal notice of allowance is thus respectfully requested.

Please apply the 2-Month Extension of Time Fee, along with any additional necessary charges or credits, to Deposit Account No. 06 1050.

Respectfully submitted,

Date: Aug. 14, 2006



William E. Hunter
Reg. No. 47,671
Attorneys for Intel Corporation

PTO Customer No. 20985
Fish & Richardson P.C.
12390 El Camino Real
San Diego, California 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

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